



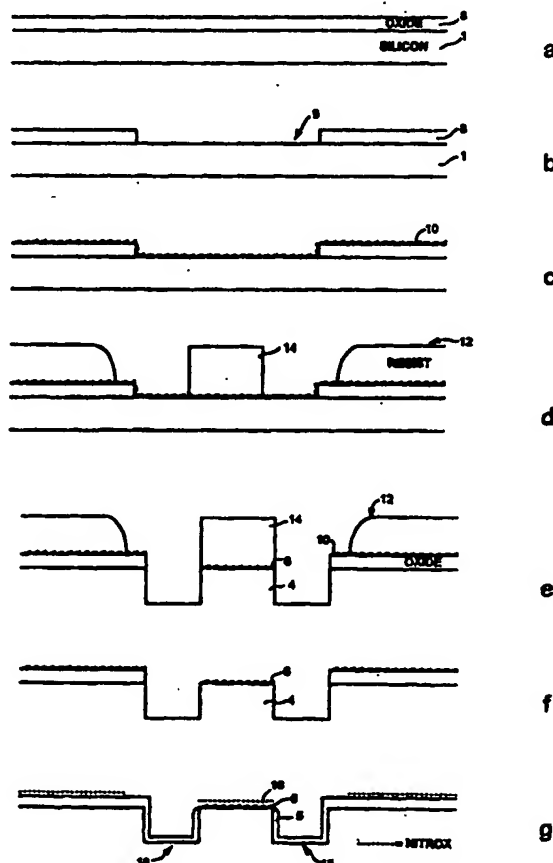
INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification ⁷ : G02B 6/12	A1	(11) International Publication Number: WO 00/25156 (43) International Publication Date: 4 May 2000 (04.05.00)
<p>(21) International Application Number: PCT/GB99/01643</p> <p>(22) International Filing Date: 25 May 1999 (25.05.99)</p> <p>(30) Priority Data: 98233133 23 October 1998 (23.10.98) GB</p> <p>(71) Applicant: BOOKHAM TECHNOLOGY LIMITED [GB/GB]; 90 Milton Park, Abingdon, Oxfordshire OX14 4RY (GB).</p> <p>(72) Inventors: DRAKE, John, Paul; 47 Rockfel Road, Lambourn, Berkshire RG17 8NG (GB). SHAW, Matthew, Peter; 44 Wytham Street, Oxford, Oxfordshire OX1 4TS (GB).</p> <p>(74) Agents: DRIVER, Virginia, Rozanne et al.; Page White & Farrer, 54 Doughty Street, London WC1N 2LS (GB).</p>	<p>(81) Designated States: AE, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CU, CZ, DE, DK, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, UA, UG, UZ, VN, YU, ZA, ZW, ARIPO patent (GH, GM, KE, LS, MW, SD, SL, SZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG).</p> <p>Published <i>With international search report.</i></p>	

(54) Title: **MANUFACTURE OF A SILICON WAVEGUIDE STRUCTURE**

(57) Abstract

A process for making a silicon rib waveguide structure is described comprising the following steps: (i) forming a window in a protective layer on the surface of a silicon wafer to expose a part of said surface; (ii) depositing a buffer layer at least over said exposed surface; (iii) carrying out an etch step to etch the buffer layer and silicon outside a protected rib portion thereby to form a silicon rib with the buffer layer on its upper surface; and (iv) forming a layer of cladding at least on side walls of the silicon rib.



FOR THE PURPOSES OF INFORMATION ONLY

Codes used to identify States party to the PCT on the front pages of pamphlets publishing international applications under the PCT.

AL	Albania	ES	Spain	LS	Lesotho	SI	Slovenia
AM	Armenia	FI	Finland	LT	Lithuania	SK	Slovakia
AT	Austria	FR	France	LU	Luxembourg	SN	Senegal
AU	Australia	GA	Gabon	LV	Latvia	SZ	Swaziland
AZ	Azerbaijan	GB	United Kingdom	MC	Monaco	TD	Chad
BA	Bosnia and Herzegovina	GE	Georgia	MD	Republic of Moldova	TG	Togo
BB	Barbados	GH	Ghana	MG	Madagascar	TJ	Tajikistan
BE	Belgium	GN	Guinea	MK	The former Yugoslav Republic of Macedonia	TM	Turkmenistan
BF	Burkina Faso	GR	Greece	ML	Mali	TR	Turkey
BG	Bulgaria	HU	Hungary	MN	Mongolia	TT	Trinidad and Tobago
BJ	Benin	IE	Ireland	MR	Mauritania	UA	Ukraine
BR	Brazil	IL	Israel	MW	Malawi	UG	Uganda
BY	Belarus	IS	Iceland	MX	Mexico	US	United States of America
CA	Canada	IT	Italy	NE	Niger	UZ	Uzbekistan
CF	Central African Republic	JP	Japan	NL	Netherlands	VN	Viet Nam
CG	Congo	KE	Kenya	NO	Norway	YU	Yugoslavia
CH	Switzerland	KG	Kyrgyzstan	NZ	New Zealand	ZW	Zimbabwe
CI	Côte d'Ivoire	KP	Democratic People's Republic of Korea	PL	Poland		
CM	Cameroon	KR	Republic of Korea	PT	Portugal		
CN	China	KZ	Kazakhstan	RO	Romania		
CU	Cuba	LC	Saint Lucia	RU	Russian Federation		
CZ	Czech Republic	LI	Liechtenstein	SD	Sudan		
DE	Germany	LK	Sri Lanka	SE	Sweden		
DK	Denmark	LR	Liberia	SG	Singapore		
EE	Estonia						

MANUFACTURE OF A SILICON WAVEGUIDE STRUCTURE

The present invention relates to manufacture of a silicon waveguide structure.

In integrated optical circuits, a silicon waveguide structure typically comprises a rib formed in the upper epitaxial silicon layer of a silicon-on-insulator chip. The rib has a top surface and side walls, and has trough portions on either side of it. The rib serves to confine an optical transmission mode for light which is contained in the rib and under the trough portions.

It is often desirable to modify the basic waveguide structure to perform a number of different functions. During these modifications, it is frequently required to treat the top surface of the rib in a manner differently to that of the side walls.

It is an aim of the present invention to provide a process for making a silicon waveguide structure which permits these modifications to be carried out in an accurately controlled fashion. Therefore it is important that however the top and side walls are individually protected, this is done in a well-aligned fashion.

According to one aspect of the invention there is provided a process for making a silicon rib waveguide structure comprising:

- forming a window in a protective layer on the surface of a silicon wafer to expose a part of said surface;

- depositing a buffer layer at least over said exposed surface;

- carrying out an etch step to etch the buffer layer and silicon outside a protected rib portion thereby to form a silicon rib with the buffer layer on its upper surface; and

- forming a layer of cladding at least on side walls of the silicon rib.

Preferred and optional features of the invention will be apparent

from the subsidiary claims of the specification.

For a better understanding of the present invention and to show how the same may be carried into effect, reference will now be made by way of example to the accompanying drawings in which:..

Figure 1 is a cross-sectional view of a known rib waveguide formed in a silicon-on-insulator chip;

Figure 2 is a perspective view of a waveguide structure;

Figures 3a to 3g are steps in a process for forming a waveguide structure; and

Figure 4 is a cross-section through a polariser.

The rib waveguide described herein is based on a silicon-on-insulator chip. A process for forming this type of chip is described in a paper entitled "Reduced defect density in silicon-on-insulator structures formed by oxygen implantation in two steps" by J. Morgail et al, Applied Physics Letters, 54, page 526, 1989. This describes a process for making silicon-on-insulator wafer. The silicon layer of such a wafer is then increased, for example by epitaxial growth, to make it suitable for forming the basis of the integrated waveguide structure described herein. Figure 1 shows a cross-section of an optical waveguide formed on such a chip. The chip comprises a layer of silicon 1 which is separated from the silicon substrate 2 by a layer of silicon dioxide 3. The rib waveguide 4 is formed in the silicon layer 1. Figure 1 also shows an oxide cladding 5 formed over the rib waveguide 4. Further details of this form of waveguide are given in a paper entitled "Low loss single mode optical waveguides with large cross-section in silicon-on-insulator" by J. Schmidtchen et al in Electronic Letters, 27, page 1486, 1991 and in PCT Patent Specification No. WO95/08787.

This form of waveguide provides a single mode, low loss (typically less than 0.2 dB/cm for the wavelength range 1.2 to 1.6 microns) waveguide typically having dimensions in the order of 3 to 5 microns which can be coupled to optical fibres and

which is compatible with other integrated components. This form of waveguide can also be easily fabricated from conventional silicon-on-insulator wafers (as described in W095/08787 referred to above) and so is relatively inexpensive to manufacture.

Figure 2 shows a perspective view of such a rib waveguide which has formed on a part of its upper surface a buffer layer 6. The buffer layer 6 typically has a length of 3 mm or less or preferably 1 mm or less.

As will become clearer in the following, the buffer layer has a number of different possible functions, in particular because the process described herein ensures that the edges of the buffer layer 6 are self-aligned with the top of the rib waveguide 4. This allows the cladding layer 5 to protect the side walls of the rib 4 while the buffer layer 6 protects its top surface. This allows for example the manufacture of a polariser by depositing a light absorbing layer on top of the buffer layer 6 but not on the side walls of the rib 4.

Moreover, if the buffer layer and the cladding layer have different etch characteristics, it allows the top surface of the rib 4 to be exposed while the side surfaces remain protected, or *vice versa* to allow selective introduction of dopants either into the top of the waveguide or through its sides. This can be done for example to control the refractive index of portions of the waveguide.

A process for making the rib waveguide of Figure 2 will now be described with reference to Figure 3.

Figure 3a shows the upper surface of a silicon-on-insulator chip, and in particular shows the silicon layer 1. A protective layer of oxide 8 having a thickness of about 7000Å is formed on the top of the silicon layer 1. Using a mask (not shown), a window 9 is etched through the oxide layer 8 to expose the surface of the silicon layer 1 (Figure 3b). A thin buffer layer 10 is then

deposited. The buffer layer is of nitride and is deposited using an LPCVD (low pressure chemical vapour deposition) process. For example, the thickness of the buffer layer may be around 170Å (see Figure 3c).

Then, according to Figure 3d, a pattern of photoresist 12 is deposited. Of importance, a central part 14 of the photoresist defines the area where the rib waveguide 4 is to be formed.

Then, an etch step is carried out to etch through the buffer layer 10 and into the silicon layer 1 to define the rib 4. This can be done as a single etch step using a known dry etch process, or as a two step etch process. This is illustrated in Figure 3e. The depth of the waveguide is for example 1.45µm.

Then, according to Figure 3f, the resist pattern 12 is removed to have the effect of leaving a buffer layer 6 perfectly aligned with the side walls of the rib 4.

Finally, an oxidation step is performed to form the cladding layer 5. The thickness of the oxide layer forming the cladding layer 5 is about 0.35 µm. During the oxidation process, the nitride layer 6 on top of the rib 4 effectively inhibits oxidation on the top surface of the rib. Only a very thin oxide layer of about 40Å will form. This is denoted 16.

Figure 4 is a cross-section through a polariser which has been formed using the rib waveguide structure made by the process described above. After the step illustrated in Figure 3g, a short oxide etch is performed which removes the native oxide layer 16 above the buffer layer 6, but still retains a significant thickness of the cladding layer 5. Then, a light absorbing layer 7 is deposited on top of the buffer layer 6. The alignment of this layer 7 is less important because the sides of the rib are protected by the silicon dioxide. The light absorbing layer 7 is preferably a metallic layer, for example aluminium. The metallic layer 7 causes attenuation of the light

received from the waveguide. More details concerning operation of a polariser of this type are given in our British Patent Application No. 9718346.1.

Another use of the structure illustrated in Figure 3g is to allow selective introduction of dopant into the rib waveguide structure. For example, if dopants are required to be introduced through the side walls or in the trough portions 18 on either side of the rib 4, then the cladding layer 5 can be etched away using an oxide etch, while the buffer layer 6 remains to protect the top surface of the rib 4. Conversely, if dopants are required to be introduced into the top surface of the rib but not into the side walls or trough portions 18, then a selective etchant can be used to etch away the nitride but leave the cladding layer 5 intact. Thus, the selective etch characteristics of the cladding layer and buffer layer allow a number of different doping possibilities.

As an alternative to the use of nitride for the buffer layer, a native oxide layer may be used. That is, during the step illustrated in Figure 3c, an oxide growth step is performed to grow a thin oxide layer on the exposed surface of the silicon layer 1 in the window 9. Afterwards, the steps are the same as already described. It can be seen that the effect of this would be to have, in the structure of Figure 3g, a slightly thicker oxide layer on the top portion of the rib as opposed to the cladding layer 5 on the side portions and trough portions. Once again however this allows for a selective etch characteristic, because for a given etch time, only a certain thickness of oxide will be removed. Therefore, it is possible to remove, for example, oxide from the side walls of the rib without removing all the oxide from the top portion.

If a native oxide layer is used, this may have, for example, a thickness of about 30Å.

Therefore, overall the buffer layer may have a thickness in the

range 20-500Å and preferably in the range 80-220Å. When considering the use of the buffer layer in a polariser, the thickness of the layer depends on the refractive index of the buffer layer.

By use of a buffer layer on the top of the rib, a pattern can be etched into the top of the rib without affecting the side walls.

CLAIMS:

1. A process for making a silicon rib waveguide structure comprising:
 - forming a window in a protective layer on the surface of a silicon wafer to expose a part of said surface;
 - depositing a buffer layer at least over said exposed surface;
 - carrying out an etch step to etch the buffer layer and silicon outside a protected rib portion thereby to form a silicon rib with the buffer layer on its upper surface; and
 - forming a layer of cladding at least on side walls of the silicon rib.
2. A process according to claim 1, wherein the buffer layer comprises silicon nitride.
3. A process according to claim 2, wherein the buffer layer is deposited using an LPCVD process.
4. A process according to claim 1, wherein the buffer layer is a native oxide.
5. A process according to any preceding claim, wherein the thickness of the buffer layer is in the range 20-500Å and preferably in the range 80-220Å.
6. A process according to any preceding claim, which further comprises the step of forming a light absorbing layer on the buffer layer to define a polariser.
7. A process according to any preceding claim, wherein the step of forming a layer of cladding comprises carrying out an oxidation step such that a cladding layer of oxide is formed on the side walls of the silicon rib.
8. A process according to any preceding claim, wherein the

cladding layer and the buffer layer have different etch characteristics.

9. A process according to any preceding claim, which further comprises selectively removing either the buffer layer from the top surface of the rib or the cladding layer from at least one of the side walls of the rib, and introducing dopants into the area from which the buffer layer or cladding layer respectively has been removed.

10. A process for making a silicon rib waveguide substantially as herein described with reference to the drawings.

1 / 3

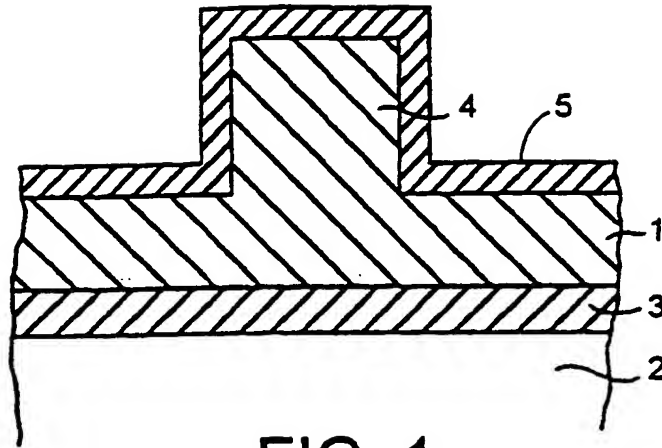


FIG. 1

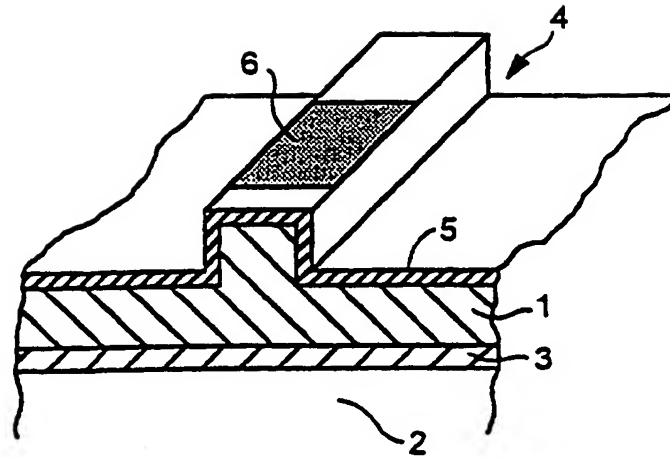


FIG. 2

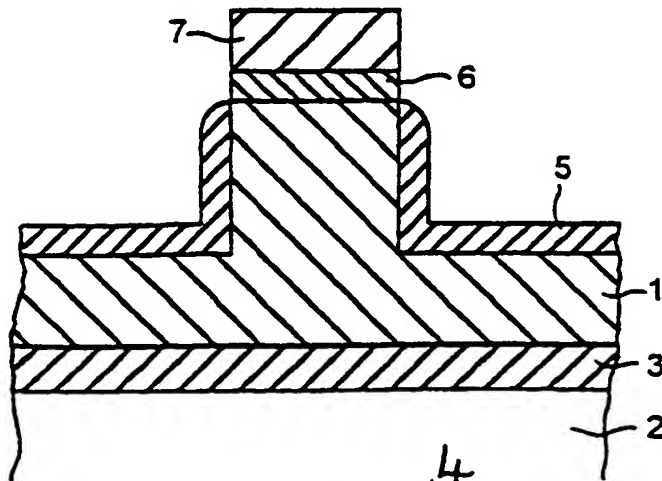
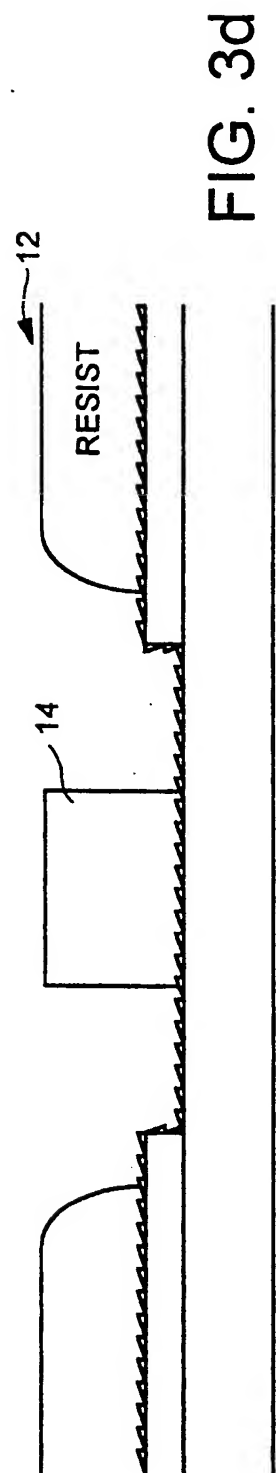
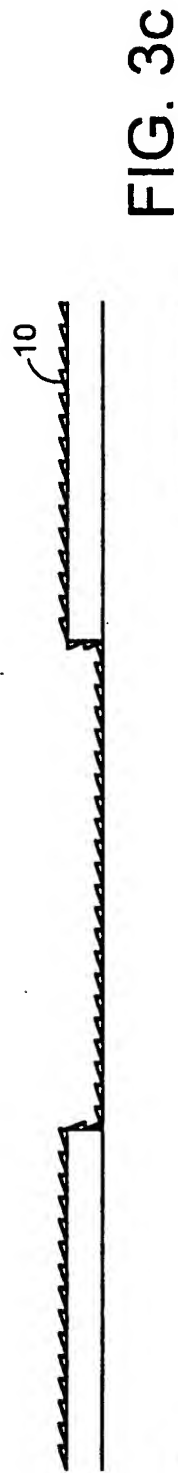
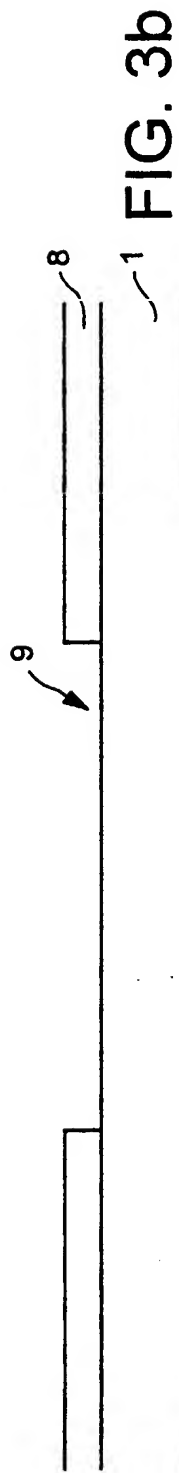
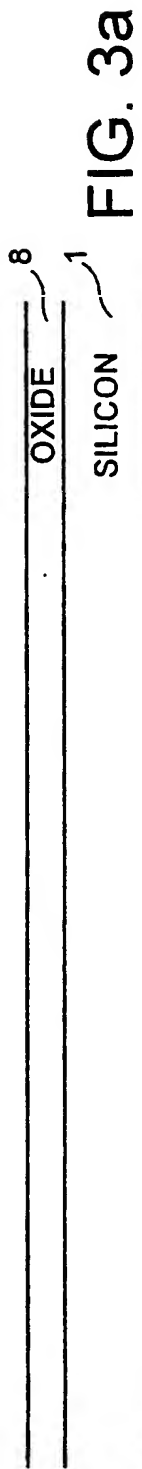


FIG. 3



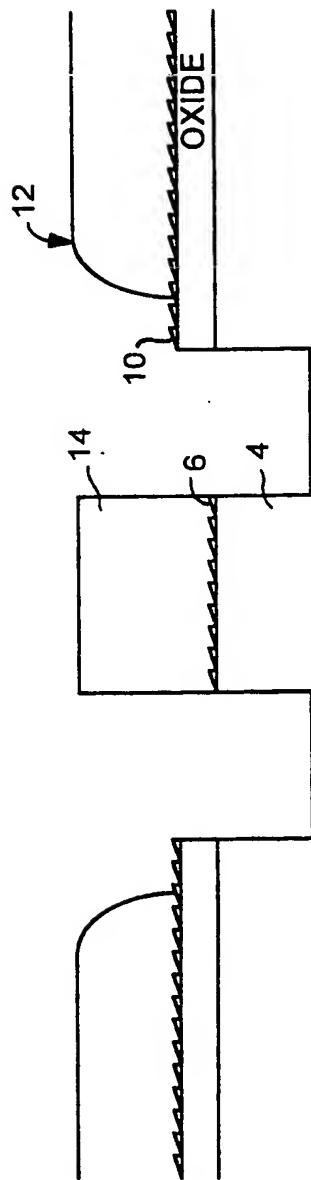


FIG. 3e

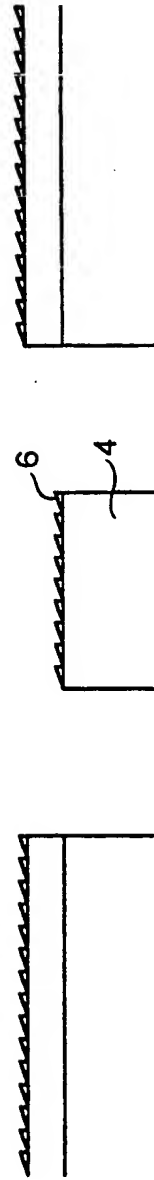


FIG. 3f

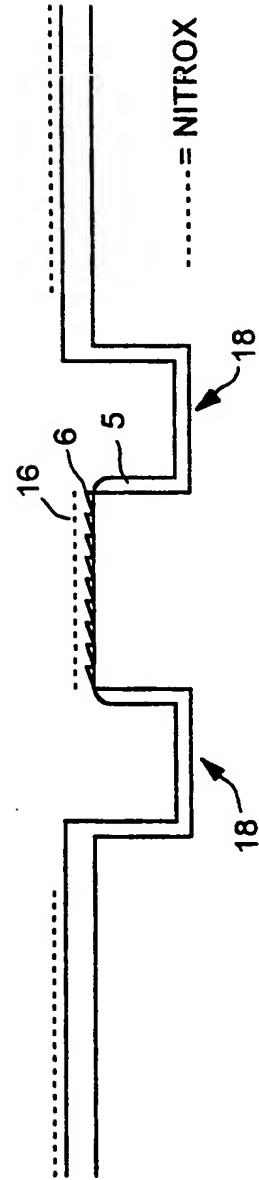


FIG. 3g

INTERNATIONAL SEARCH REPORT

International Application No

PCT/GB 99/01643

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 G02B6/12

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 G02B

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	GB 2 318 647 A (BOOKHAM TECHNOLOGY LTD) 29 April 1998 (1998-04-29) cited in the application abstract; figures 1-3 page 1	1-10
A	WO 95 08787 A (BOOKHAM TECHNOLOGY LTD ; CRAMPTON STEPHEN JAMES (GB); HARPIN ARNOLD) 30 March 1995 (1995-03-30) cited in the application abstract; figures 2,4 page 4 - page 5	1-10
A	US 5 483 609 A (NAKAYA KEN-ICHI) 9 January 1996 (1996-01-09) abstract; figures 4B,6C	1-10
	-/-	

☒ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search

25 August 1999

Date of mailing of the international search report

01/09/1999

Name and mailing address of the ISA

European Patent Office, P.B. 5818 Patentlaan 2
NL - 2280 HV Rijswijk
Tel. (+31-70) 340-2040, Tx. 31 651 epo nl,
Fax: (+31-70) 340-3016

Authorized officer

Jakober, F

INTERNATIONAL SEARCH REPORT

International Application No

PCT/GB 99/01643

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	EP 0 433 552 A (IBM) 26 June 1991 (1991-06-26) abstract; figures 1,2 -----	1-10

Information on patent family members

International Application No

PCT/GB 99/01643

Patent document cited in search report		Publication date	Patent family member(s)	Publication date
GB 2318647	A	29-04-1998	AU 8817198 A	22-03-1999
			WO 9912062 A	11-03-1999
WO 9508787	A	30-03-1995	DE 69315359 D	02-01-1998
			DE 69315359 T	10-06-1998
			EP 0720754 A	10-07-1996
			JP 9503869 T	15-04-1997
			US 5757986 A	26-05-1998
US 5483609	A	09-01-1996	JP 7028007 A	31-01-1995
EP 0433552	A	26-06-1991	US 4997246 A	05-03-1991
			JP 2681044 B	19-11-1997
			JP 3196120 A	27-08-1991